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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,764	10/22/2001	Kohji Kanamori	N32565600	5751

7590

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EXAMINER

FOURSON III, GEORGE R

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 04/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/032,764

Applicant(s)

KANAMORI, KOHJI

Examiner

George Fourson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspond nc address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 03 February 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 1-7 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 8-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

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The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 8,9,12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Bois, Japanese Patent 62-216268 and Kwon.

The rejection is maintained as stated in the paper mailed 11/1/02 and as restated below.

Bois discloses formation of LOCOS mask 4, exemplifying silicon nitride, local oxidation of the substrate to produce a LOCOS film 8, etching of 8 using mask 4 to form trench 10, filling of trench 10 with dielectric 14 and planarization of dielectric 14 to the level of LOCOS film 8. The reference does not disclose use of a conductive layer in the LOCOS mask or the use of sidewalls on mask 4 to etch trench 10.

Japan '268 discloses LOCOS using a nitride 4/conductive film 3/oxide film 2. It would have been within the scope of one of ordinary skill in the art to combine the teachings of Bois and Japan '268 to enable formation of the LOCOS mask of Bois.

Kwon discloses formation of trench 8 through LOCOS film 5A by formation of sidewalls 6A on LOCOS mask nitride 4/polysilicon 3/oxide 2 (fig.1A-1C). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Bois and Kwon to enable formation of trench 10 of Bois.

Choice of particular thickness of the LOCOS film would have been within the scope of one of ordinary skill in the art as a matter of routine optimization.

Applicant argues that there is no stated motivation to combine the teachings of Bois and Japan '268. However, the motivation is stated above and in the paper mailed 11/1/02 to be "It would have been within the scope of one of ordinary skill in the art to combine the teachings of Bois and Kwon to enable

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formation of trench 10 of Bois". Art recognized suitability for an intended purpose has been recognized as motivation to combine. MPEP 2144.07. Japan '268 discloses formation of a mask that is disclosed to be suitable in LOCOS processes such as is performed in the process of Bois.

Applicant argues that the references teach away from the proposed modification pointing to the additional teaching of Japan '268 that a remaining patterned portion of the LOCOS mask can be employed as a gate electrode. However, the additional pointed to teaching does not negate those relied on, namely local oxidation of silicon to form a field oxide using a nitride 4/conductive film 3/oxide film 2 mask.

Applicant argues that there is no stated motivation to combine the teachings of Bois and Japan '268 with those of Kwon. However, the motivation is stated above and in the paper mailed 11/1/02 to be "It would have been within the scope of one of ordinary skill in the art to combine the teachings of Bois and Kwon to enable formation of trench 10 of Bois.". Art recognized suitability for an intended purpose has been recognized as motivation to combine. MPEP 2144.07. Kwon discloses a process as suitable in forming a trench through a LOCOS film such as is performed in the process of Bois.

Applicant argues that advantages are associated with the recited LOCOS film thickness and that such advantages are unexpected. However, applicant has merely recognized properties of the process made obvious by the combination of references discussed above. Further, the allegation of unexpected results is not persuasive in the absence of objective evidence. MPEP 716.02.

Applicant argues that claim 13 has not been addressed. In response any of the film layers of the stacked film could perform the recited function of providing a stopper for a CMP step.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Bois, Japanese Patent 62-216268 and Kwon as applied to claims 8,9,12 and 13 above, and further in view of Lai.

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The rejection is maintained as stated in the paper mailed 11/1/02 and as restated below.

The combination does not include forming a dielectric on the conductive layer or another conductor layer on the dielectric layer. Lai discloses forming an EEPROM which includes forming an insulator on a polysilicon layer and a further polysilicon layer. It would have been within the scope of one of ordinary skill in the art to combine the teachings of the combination and those of Lai to enable EEPROM formation.

Applicant argues that there is no stated motivation to combine the teachings of Bois, Japan '268, and Kwon with those of Lai. However, the motivation is stated above and in the paper mailed 11/1/02 to be "It would have been within the scope of one of ordinary skill in the art to combine the teachings of the combination and those of Lai to enable EEPROM formation.". However, art recognized suitability for an intended purpose has been recognized as motivation to combine. MPEP 2144.07. The process of the combination teaches formation of layers corresponding to a gate oxide and floating gate according to the teachings of Lai. The formation of a control gate on such a structure is disclosed by Lai.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Bois, Japanese Patent 62-216268 and Kwon as applied to claims 8,9,12 and 13 above, and further in view of either one of Rho et al or Suh et al, newly cited.

The rejection is maintained as stated in the paper mailed 11/1/02 and as restated below.

The combination does not include forming the sidewalls using nitride. The examiner takes official notice that formation of nitride spacers as part of a hard mask was known prior to applicant's invention. It

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would have been within the scope of one of ordinary skill in the art to combine the known process with that of the combination to enable formation of the mask used to etch the LOCOS film.

Applicant requests provision of evidence supporting the taking of official notice. In response, Rho et al discloses trench etching by formation of a nitride sidewall 34 on nitride 33/oxide 32 mask. Suh discloses trench etching by formation of nitride sidewall 304 on nitride 303/oxide 302 mask. It would have been within the scope of one of ordinary skill in the art to combine the teachings of Bois, Japanese Patent 62-216268 and Kwon with the teachings of either one of Rho et al or Suh et al to enable formation of the spacers of the combination.

Claims 14 and 15 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Bois.

The rejection is maintained as stated in the paper mailed 11/1/02.

Applicant argues that no reasons or grounds for motivation have been provided. In response applicant is directed to the statement "Claims 14 and 15 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Bois". No explanation is necessary because the entire patent is directed to the claimed subject matter including the abstract and all figures. In the interest of compact prosecution applicant is directed to the statements regarding the reference above.

Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bois as applied to claims 14 and 15 above, and further in view of Lai.

The rejection is maintained as stated in the paper mailed 11/1/02 and as restated below.

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Bois discloses removal of the LOCOS mask and formation of MOS IC devices including transistors (col.1, lines 7-15). The reference does not disclose formation of a gate oxide and a gate on the substrate between the LOCOS films and overlapping a portion of the films.

Lai teaches provision of an EEPROM between and overlapping LOCOS regions (fig.5). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Bois and Lai to enable EEPROM formation as the device formation step of Bois.

Applicant argues that no reasons or grounds for motivation have been provided. In response applicant is directed to the statement "Claims 14 and 15 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Bois". No explanation is necessary because the entire patent is directed to the claimed subject matter including the abstract and all figures. In the interest of compact prosecution applicant is directed to the statements regarding the reference above.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

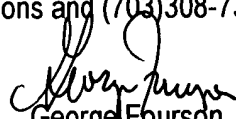
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956. See MPEP 203.08.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner George Fourson whose telephone number is (703) 308-2544. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794. The fax number for this group is (703)308-7722 (or extensions 7724, 3431 or 3432) for regular communications and (703)308-7382 for after final communications.

  
George Fourson  
Primary Examiner  
Art Unit 2823

GFourson  
April 17, 2003